REMARKS

Applicants respectfully request the present application be reconsidered.

An Office Action mailed on November 2, 2006 ("Office Action"), rejected Claims 1-4 and 16. The Office Action also objected to Claim 3 for informalities. The Office Action rejected Claims 1-4 and 16 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,784,630 issued to Saito et al. ("Saito et al."). Claims 1, 2, and 16 have been amended to more clearly distinguish them over the cited reference and further clarify claim language. Claim 3 has been amended to overcome the objection.

Applicants have carefully considered the arguments of the Examiner in the Office Action and respectfully submit that the amended claims pending in the present application are allowable for the reasons set forth below.

Allowability of Claims 1-4 and 16 Under 35 U.S.C. § 103(a)

As noted above, Claims 1-4 and 16 were rejected under 35 U.S.C. § 103 as being unpatentable over Saito et al. Applicants respectfully disagree for the reasons set forth below.

Amended independent Claim 1 recites, in its entirety:

> 1. A multi-port instruction/data integrated cache which is provided between a parallel processor to execute a plurality of types of processing in one clock cycle and a main memory and which stores a part of instructions and data stored in the main memory, comprising:
>
> a plurality of memory banks;
>
> a plurality of ports including an instruction port unit consisting of at least one instruction port used to access an instruction from the parallel processor, and a data port unit consisting of at least one data port used to access data from the parallel processor, and
>
> the data port and the instruction ports are connected individually to at least one predetermined memory bank,

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wherein a number of memory banks connected to the data port is larger than a number of memory banks connected to the instruction ports,

wherein a data width specified between the memory bank and the instruction port is larger than a data width specified between the memory bank and the data port. (Emphasis added.)

Saito et al. does not teach or suggest a data port and an instruction port connected individually to at least one predetermined bank, wherein a *number of memory banks connected to the data port is larger than the number of banks connected to the instruction port*. Saito et al. discloses cache memory having cache memory banks 14-1 through 14-n each having one read port and one write port. Saito et al. further discloses that the cache memory banks 14-j are connected to the bank/decision circuit 16, which in turn is connected to the data selector circuits 18-i. The data selector circuits 18-i are connected to the processor 20-i via the data line 110-i. (Col. 31, lines 1-17.) Saito et al. does not disclose the connection between multiple memory banks and multiple ports, much less disclosing a number of memory banks connected to the data port that is larger than a number of memory banks connected to the instruction ports, as recited in amended Claim 1.

Saito et al. does not teach or suggest a data width specified between the memory bank and the instruction port is larger than a data width specified between the memory bank and the data port. With reference to Figure 1, Saito et al. discloses that "a cache controller which serves to *change or modify* the *width and the number of data* read out from or written in the cache memory A5 in accordance with the values set at the parallelism flag A7" (Col. 8, lines 55-59; emphasis added). Therefore, Saito et al. discloses that data width of each port is dynamically changed according to the progress of the program being executed and the state of the parallelism flag A7. The dynamic changing of the data width necessitates that each of the end ports of the cache memory A5 be physically connected to all cache banks. This is in contrast to amended Claim 1 which recites that a data width specified between the memory bank and the instruction

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port is larger than a data width specified between the memory bank and the data port. Therefore, amended independent Claim 1 is submitted to be allowable for at least the reasons discussed above.

Claims 2-4 depend from Claim 1 and are submitted to be allowable for at least the same reasons discussed above with respect to Claim 1.

Amended independent Claim 16 recites, in relevant portions, the same features recited in amended independent Claim 1. More specifically, Claim 16 recites, *inter alia*, "wherein each *data width* specified *between the memory bank and the instruction port and the trace port is larger than a data width* specified *between the memory bank and the data port*" (emphasis added). Saito et al. does not teach or suggest a trace cache or a trace port. Saito et al. discloses control instructions, such as a *test-and-set or compare-and-swap instruction* issued for a specific address of the main memory. Saito et al. further discloses that the compare-and-swap instruction is intended to mean such instruction which is executed for reading out data from a memory, checking the value of the data read out, and writing the data in the memory at the original address. (Col. 16, lines 41-49.) Test-and-set or compare-and-swap instructions are not the same as trace data. Those skilled in the art will appreciate that trace data are a sequence of instructions executed by a processor typically used in debugging software programs. In contrast, instructions such as test-and-set or compare-and-swap are individual instructions included in a processor instruction set. An individual instruction does not constitute a trace. Additionally, Saito et al. does not teach or suggest that a data width specified between the memory bank and the instruction port and the trace port is larger than a data width specified between the memory bank and the data port, as recited in amended independent Claim 16. As noted above with respect to Claim 1, Saito et al. discloses a cache controller A6 which serves to change or modify the width and the number of data read out from or written in the cache memory according to the

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parallelism flag A7, necessitating each of the ports of the cache memory A5 be physically connected to all memory banks of the cache memory A5. Therefore, amended independent Claim 16 is submitted to be allowable for at least the reasons discussed above.

CONCLUSION

In view of the foregoing amendments and remarks, applicants submit that the present application is in condition for allowance. Early action to that end is respectfully requested. Should any issues remain needing resolution prior to allowance, the Examiner is invited to contact applicants' attorney at the telephone number indicated below.

Respectfully submitted,

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